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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/675,462	09/30/2003	Andrew Jarabek	PAT 2513-2 US	5556

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EXAMINER	
HAN, CLEMENCE S	

ART UNIT	PAPER NUMBER
2416	

NOTIFICATION DATE	DELIVERY MODE
01/26/2009	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No.	Applicant(s)	
	10/675,462	JARABEK ET AL.	
	Examiner	Art Unit	
	CLEMENCE HAN	2416	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 September 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *2-15 and 17-27* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *2-14,17-22 and 24-27* is/are rejected.

7)☒ Claim(s) *15 and 23* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claim 2-9, 13, 14 17-19, 21, 22 and 24-26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mochizuki (US Pub. 2003/0053494) in view of Bosshart (US Pub. 2004/0022239).

Regarding claim 7 and 18, Mochizuki teaches a method of processing an output signal comprising: checking a state of a control bit (STS/VT SEL in Figure 4) that specifies whether to assemble an output signal from multiple virtual tributary (VT) or tributary unit (TU) connections or handle the output signal as an synchronous transport signal (STS) or administrative unit (AU) connection [0056]; switching a predetermined number of entries together based on the state of the control bit [0062]. Mochizuki, however, does not explicitly disclose storing the control bit in a connection memory. Bosshart teaches storing connection pattern in a connection memory 12 in a SONET system [0023]. It would have been obvious to one skilled in the art modify Mochizuki to store the control bit in a connection memory as taught by Bosshart in order to output to the desired output channel [0023].

Regarding claim 2 and 17, Mochizuki teaches the control bit (STS/VT SEL in Figure 4) is set by a programmer (STS/VT SEL is the information programmed to designate the STS signal or the VT signal [0056].

Regarding claim 3, Mochizuki teaches handling the output signal as an STS connection when the control bit (STS/VT SEL in Figure 4) is set ([0062], also see Figure 5).

Regarding claim 4, Mochizuki teaches assembling the output signal from multiple VT/TU connections when the control bit (STS/VT SEL in Figure 4) is not set ([0062], also see Figure 5).

Regarding claim 5, Mochizuki teaches handling the output signal as the AU connection when the control bit (STS/VT SEL in Figure 4) is not set ([0062], also see Figure 5).

Regarding claim 6, Mochizuki teaches assembling the output signal from multiple VT connections when the control bit (STS/VT SEL in Figure 4) is set ([0062], also see Figure 5).

Regarding claim 8 and 19, Bosshart teaches storing the control bit in a register 12.

Regarding claim 9, Mochizuki teaches checking a state of a second control bit (STS COUNTER in Figure 5).

Regarding claim 13 and 21, Bosshart teaches storing the second control bit in a connection memory 12.

Regarding claim 14 and 22, Bosshart teaches storing the second control bit in a register 12.

Regarding claim 24, Mochizuki teaches an apparatus for processing an output signal comprising: a control bit (STS/VT SEL in Figure 4) that specifies whether to assemble the output signal from multiple virtual tributary (VT) connections or handle the output signal as an synchronous transport signal (STS) or administrative unit (AU) connection [0056]; a circuit 10 to check a state of the control bit [0070]; and control circuitry that uses a second memory to switch a predetermined number of entries together based on the state of the control bit [0062]. Mochizuki, however, does not explicitly disclose the control bit in a first memory. Bosshart teaches storing connection pattern in a memory 12 in a SONET system [0023]. It would have been obvious to one skilled in the art modify Mochizuki to store the control bit in a memory as taught by Bosshart in order to output to the desired output channel [0023].

Regarding claim 25, Mochizuki teaches the control circuitry is configured to handle the output signal as an STS connection when the control bit (STS/VT SEL in Figure 4) is set ([0062], also see Figure 5).

Regarding claim 26, Mochizuki teaches the control circuitry is configured to assemble the output signal from multiple VT connections when the control bit (STS/VT SEL in Figure 4) is not set ([0062], also see Figure 5).

3. Claim 10-12, 20 and 27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mochizuki (US Pub. 2003/0053494) in view of Bosshart (US Pub. 2004/0022239) and further in view of Miller (US Pub. 2004/0100994).

Regarding claim 10 and 20, Mochizuki teaches the second control bit (STS COUNTER in Figure 5). Mochizuki in view of Bosshart, however, does not teach the second control bit is associated with independent and concatenated payloads. Miller teaches second control bit (V1, V2 in Figure 2) is associated with independent and concatenated payloads [0026]. It would have been obvious to one skilled in the art to modify Mochizuki in view of Bosshart to have second control bit associated with independent and concatenated payload as taught by Miller in order to process superframes [0026].

Regarding claim 11, Mochizuki teaches cross-connecting a second payload with a first payload if the second control bit (V1, V2 in Figure 2) is set [0026].

Regarding claim 12, Mochizuki teaches cross-connecting a second payload with a first payload if the second control bit (V1, V2 in Figure 2) is not set [0026].

Regarding claim 27, Mochizuki teaches the second control bit (STS COUNTER in Figure 5). Mochizuki in view of Bosshart, however, does not teach the first memory stores a second control bit that specifies whether payloads are independent or concatenated, and the control circuit is configured to switch a predetermined number of payloads together based on a state of the second control bit. Miller teaches the first memory stores a second control bit (V1, V2 in Figure 2) that specifies whether payloads

are independent or concatenated, and the control circuit is configured to switch a predetermined number of payloads together based on a state of the second control bit [0026]. It would have been obvious to one skilled in the art to modify Mochizuki in view of Bosshart to have second control bit associated with independent and concatenated payload as taught by Miller in order to process superframes [0026].

Allowable Subject Matter

4. Claim 15 and 23 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

5. Applicant's arguments with respect to claim 2-15 and 17-27 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to CLEMENCE HAN whose telephone number is (571)272-3158. The examiner can normally be reached on Monday-Friday 8-4.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ricky Ngo can be reached on (571) 272-3139. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Ricky Ngo/
Supervisory Patent Examiner, Art Unit 2416

/C. H./
Examiner, Art Unit 2416